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| 09/528,524 | 03/20/2000 | Jacques Michelet | B-3881-617765-1 | 5142 |

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| EXAMINER | |
|---|---|
| HUYNH, LUAT T | |
| ART UNIT | PAPER NUMBER |
| 2121 | |

DATE MAILED: 12/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/528,524 | MICHELET ET AL. | |
| | Examiner | Art Unit | |
| | Luat (Luke) T. Huynh | 2121 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Appeal Brief*

1. Applicant's arguments with respect to claims 1, 6, and 15 have been considered but are moot in view of the new ground(s) of rejection. Therefore, the finality from the previous office action has been withdrawn.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee U.S. Patent No. 5,631,698 in view of 'HP MaxiLife: for the Highest Productivity and Reliability' (hereinafter HP-MaxiLife).

As to claim 1, Lee discloses a communication process between an Information Handling System (IHS) and at least one display having On Screen Display (OSD) (see unit 240 in Fig. 1) capability wherein:

said IHS system includes a processor (see controller 200 in Fig. 1) under control of an operating system, a graphics system (see video signal processor 160 in Fig. 1);

said at least one display (col. 2, line 55) receives a graphics channel comprising the graphics signals generated by said graphics system and a service channel allowing interaction between said at least one display and said operating system;

However, Lee does not disclose that an electronic circuit operating independently of said processor and said graphics system.

HP-MaxiLife teaches the use of an electronic circuit (p. 2, line 35) operating independently of said processor and said graphics system. The independent electronic circuit uses said service channel to have access to the OSD capability of said at least one display (p. 2, lines 36-37) in order to display text and/or graphics independently of said processor and said operating system.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the hardware monitoring process having On Screen Display capability of HP-MaxiLife into the computer system of Lee in order to maximize reliability and system up-time.

As to claim 6, Lee discloses an Information Handling System (IHS) comprising all the limitations as discussed above in claim 1. Lee also discloses at least one display (col. 2, line 55) having On Screen Display (OSD) capability and including first receiving means, lines 23-26) for receiving a graphics channel upon which graphics signals generated by said graphics system are transmitted, and second receiving means for receiving a service channel allowing interaction between said at least one display and said operating system (see Fig. 1 and col. 2, lines 51-59).

As to claim 15, Lee discloses a display device having On Screen Display (OSD) capability for use in an Information Handling System (IHS) including a processor under control of an operating system, a graphics system and an electronic circuit operating independently of said processor and said graphics system, said display having one or more connectors for receiving a graphics channel comprising graphics signals generated by said graphics system and

a service channel allowing interaction between said display and said operating system as discussed above in claim 6;

characterized by means responsive to commands in said service channel for controlling the On Screen Display capability independently of the operation of the processor and the operating system (col. 2, lines 55-59).

Claims 2-3, 5, 7-9, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of HP-MaxiLife and further in view of 'VESA Display Data Channel Command Interface (DDC/CI) Standard' (hereinafter VESA).

As to claim 2, the combination of Lee/HP-MaxiLife as recited in claim 1 further fails to disclose the display consists of "*a bi-directional serial communication link which is compatible with the IC protocol, providing either DDC or DDC/CI communication support with said operating system,*" as well as an IC communication link between said independent electronic circuit and said at least one display in order to provide to said electronic circuit and a direct access to the OSD capability of said at least one display.

VESA teaches the use of DDC/CI offers bi-directional communication between the computer graphic host and the display device (see Summary on p. 1) using IC communication.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the bi-directional communication DDC/CI of VESA into the independent electronic circuit of HP-MaxiLife in order to maximize reliability and system up-time.

As to claim 3, HP-MaxiLife discloses the process according to claim 2 characterized in that said electronic circuit consists of a hardware monitoring circuit displaying monitoring feedback information to the user via said service channel (p. 4, line 12).

As to claim 5, the process according to claim 3 characterized in that said hardware monitoring circuit is connected via a network to said IHS system in order to provide an alarm on Local Area Network (LAN) capability. Although the invention has been describes with a certain degree of particularity, it should be recognized that elements thereof may be altered by persons skilled in the art by applying the monitoring circuit into a local area network when desired by the user without departing from the spirit and scope of the invention.

As to claim 7, Information Handling System according to claim 6 characterized in that said service channel consists of a bi-directional serial communication link, which VESA discloses the interaction between the display and its graphic host (see Summary on p. 9).

As to claim 8, Lee discloses an Information Handling System (IHS) as recited in claim 7 wherein said serial communication link is compatible with the IC protocol, and provides a DDC or a DDC/CI communication interface with said processor as well as a IC communication link between said independent electronic circuit and said at least one display in order to provide to said electronic circuit a direct access to the OSD capability of said at least one display, which VESA discloses DDC/CI display control interface level (p. 11).

As to claim 9, HP-MaxiLife disclose the process according to claim 7 characterized in that said electronic circuit consists of a hardware monitoring circuit displaying monitoring feedback information to the user via said service channel (p. 4, line 12).

As to claim 16, the combination of Lee/HP-MaxiLife as recited in claim 15 further fails to disclose the display consists of "*a bi-directional serial communication link which is compatible with the IC protocol, providing either DDC or DDC/CI communication with said operating system,*" as well as an IC communication link between said independent electronic circuit and said display in order to provide to said electronic circuit a direct access to the OSD capability of said display.

VESA teaches the use of DDC/CI offers bi-directional communication between the computer graphic host and the display device (see Summary on p. 1) using IC communication.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the bi-directional communication DDC/CI of VESA into the independent electronic circuit of HP-MaxiLife in order to maximize reliability and system up-time.

Claims 10-14 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of HP-MaxiLife, in view of VESA, and further in view of Fisch U.S. Patent No. 5,901,297.

As to claim 10, the Information Handling System (IHS) comprising all the limitations as discussed above in claim 8 characterized in that said graphics systems except that the combination of Lee/HP-MaxiLife/VESA fails to disclose an arbitration means having a first input connected to receive said first IC communication channel provided by said graphics engine, and having a second input for receiving a second IC communication channel provided by said hardware monitoring circuit;

said arbitration means providing arbitration between said first and said second IC communication links so that the hardware monitoring circuit and the processor can both get access to said second receiving means of said at least one display.

Fisch teaches the use of an initialization mechanism for symmetric arbitration agents (see arbitration unit 320 in Fig. 3). The arbitration counter of each bus agent is used to keep track of which agent was the last or current owner of the bus and which agent will be the next owner of the bus (col. 2, lines 35-40).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the arbitration means of Fisch into the computer system of Lee in order to improve the efficiency of the hardware monitoring systems.

As to claim 11, Lee discloses an Information Handling System (IHS) as recited in claim 10 characterized in that said graphics systems is an AGP or PCI graphics card, which is the common graphics interface that allows high performance graphics to be generated in a personal computer, plugged into a corresponding AGP or PCI graphics slot having at least two wires which are dedicated for the communication of said second IC protocol communication channel.

As to claim 12, Lee discloses an Information Handling System (IHS) as recited in claim 11 characterized in that said graphics system and said processor are located on the same motherboard. This is well known in the computer industry.

As to claim 13, Lee discloses an Information Handling System (IHS) as recited in claim 6 characterized by:

a graphics engine (see video signal processor 160 in Fig. 1) for providing graphics signals to said graphics channel and a first IC communication channel complying with the DDC/CI protocol (as discussed above by VESA) for controlling said at least one display (col. 2, line 55);

arbitration means having a first input connected to receive said first IC communication channel provided by said graphics engine, and having a second input receiving a second IC communication channel provided by said hardware monitoring circuit;

said arbitration means for providing arbitration between said first and said second IC communication channels so that both hardware monitoring circuit and said processor can get access to said second receiving means of said at least one display without contention.

Typical device such as arbiter is used in the computer industry as known to those skilled in the art. The arbiter receives requests for data from various parts of the computer system. The arbiter selects one of the requests and outputs it to the display as discussed above in claim 10.

As to claim 14, Lee discloses an Information Handling System (IHS) as recited in claim 13 characterized in that said arbitration means are arranged to prevent the access of said service channel to one among said first and second IC communication links until a preceding IC transaction has been successfully completed. This process is interpreted as an operable connection is achieved and memory status obtained by system component such as a device arbiter, tracking past memory access activities and inferring the status of one or more memory devices from that past activity.

As to claim 17, Lee discloses the graphics system for use in an Information Handling System (IHS) as recited in claim 7 characterized by:

a graphics engine (see video signal processor 160 in Fig. 1) for providing graphics signals to said graphics channel and a first IC communication channel complying with the DDC/CI protocol (as discussed above by VESA) for controlling said at least one display (col. 2, line 55);

arbitration means having a first input connected to receive said first IC communication channel provided by said graphics engine, and having a second input receiving a second IC communication channel provided by said hardware monitoring circuit;

said arbitration means for providing between said first and said second IC communication channels so that both hardware monitoring circuit and said processor can get access to said second receiving means of said at least one display without contention.

Typical device such as arbiter is used in the computer industry as known to those skilled in the art. The arbiter receives requests for data from various parts of the computer system. The arbiter selects one of the requests and outputs it to the display as discussed above in claim 10.

As to claim 18, Lee discloses the graphics system for use in an Information Handling System (IHS) as recited in claim 8 characterized by:

a graphics engine (see video signal processor 160 in Fig. 1) for providing graphics signals to said graphics channel and a first IC communication channel complying with the DDC/CI protocol (as discussed above by VESA) for controlling said at least one display (col. 2, line 55);

arbitration means having a first input connected to receive said first IC communication channel provided by said graphics engine, and having a second input receiving a second IC communication channel provided by said hardware monitoring circuit;

said arbitration means for providing between said first and said second IC communication channels so that both hardware monitoring circuit and said processor can get access to said second receiving means of said at least one display without contention.

Typical device such as arbiter is used in the computer industry as known to those skilled in the art. The arbiter receives requests for data from various parts of the computer system. The arbiter selects one of the requests and outputs it to the display as discussed above in claim 10.

As to claim 19, Lee discloses the graphics system for use in an Information Handling System (IHS) as recited in claim 9 characterized by:

a graphics engine (see video signal processor 160 in Fig. 1) for providing graphics signals to said graphics channel and a first IC communication channel complying with the DDC/CI protocol (as discussed above by VESA) for controlling said at least one display (col. 2, line 55);

arbitration means having a first input connected to receive said first IC communication channel provided by said graphics engine, and having a second input receiving a second IC communication channel provided by said hardware monitoring circuit;

said arbitration means for providing between said first and said second IC communication channels so that both hardware monitoring circuit and said processor can get access to said second receiving means of said at least one display without contention.

Typical device such as arbiter is used in the computer industry as known to those skilled in the art. The arbiter receives requests for data from various parts of the computer system. The arbiter selects one of the requests and outputs it to the display as discussed above in claim 10.

As to claim 20, Lee discloses the graphics system for use in an Information Handling System (IHS) as recited in claim 10 characterized by:

a graphics engine (see video signal processor 160 in Fig. 1) for providing graphics signals to said graphics channel and a first IC communication channel complying with the DDC/CI protocol (as discussed above by VESA) for controlling said at least one display (col. 2, line 55);

arbitration means having a first input connected to receive said first IC communication channel provided by said graphics engine, and having a second input receiving a second IC communication channel provided by said hardware monitoring circuit;

said arbitration means for providing between said first and said second IC communication channels so that both hardware monitoring circuit and said processor can get access to said second receiving means of said at least one display without contention.

Typical device such as arbiter is used in the computer industry as known to those skilled in the art. The arbiter receives requests for data from various parts of the computer system. The arbiter selects one of the requests and outputs it to the display as discussed above in claim 10.

***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,670,972 to Kim. Kim discloses a self-diagnostic arrangement for a video display apparatus and method effectuating the same.

U.S. Patent No. 5,956,022 to Cheng. Cheng discloses an interactive monitor trouble-shooting device includes a microprocessor based control unit, which detects the horizontal synchronization signal and the vertical synchronization signal from the video card of a computer.

U.S. Patent No. 5,583,491 to Kim. Kim discloses a method for displaying state of remote controller battery on a television set.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luat (Luke) T. Huynh whose telephone number is (703) 305-4562. The examiner can normally be reached on Monday-Friday, alternate Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A. Follansbee can be reached on (703) 305-8498. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

LUAT (LUKE) HUYNH
PATENT EXAMINER

lh
October 31, 2002

For John Follansbee
Ramesh Patel
RAMESH PATEL
PRIMARY EXAMINER
11/4/02